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1. Changed space to underscore

library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
use IEEE.STD\_LOGIC\_ARITH.ALL;  
use IEEE.STD\_LOGIC\_UNSIGNED.ALL;  
entity final\_prob1 is  
 Port ( k: in STD\_LOGIC;  
 p: in STD\_LOGIC;  
 s: in STD\_LOGIC;  
 w: out STD\_LOGIC);  
end final\_prob1;  
architecture Behavioral of final\_prob1 is  
begin  
 process(k, p, s, w)  
 begin  
 w <= (p AND (NOT k)) OR s;  
 end process;  
end Behavioral;

1. Added missing )

entity final\_prob2 is  
   Port ( A: in STD\_LOGIC\_VECTOR (1 DOWNTO 0);  
 B: in STD\_LOGIC\_VECTOR (1 DOWNTO 0);  
 F: out STD\_LOGIC\_VECTOR (1 DOWNTO 0));  
end final\_prob2;  
architecture Behavioral of final\_prob2 is  
begin  
 process(A, B)  
 begin  
 F <= A(0) AND B(0);  
 end process;  
end Behavioral;

1. Changed wait times

LIBRARY ieee;  
USE ieee.std\_logic\_1164.ALL;  
ENTITY TestBench IS  
END TestBench;  
ARCHITECTURE TestBenchArch OF TestBench IS  
 COMPONENT UnitUnderTest IS  
 PORT (a, b: IN std\_logic;  
 c: OUT std\_logic);  
 END COMPONENT;  
 SIGNAL x, y, z: std\_logic;  
BEGIN  
 CompToTest: UnitUnderTest PORT MAP (x, y, z);  
 PROCESS  
 BEGIN  
 x <= '0'; y <= '1';  
 WAIT FOR 10 ns;  
 x <= '1';  
 WAIT FOR 20 ns;  
 x <= '0'; y <= '0';  
 WAIT FOR 10 ns;  
 x <= '1';  
 WAIT FOR 20 ns;  
 x <= '0'; y <= '1';  
 WAIT FOR 40 ns;  
 END PROCESS;  
END TestBenchArch;

1. Added connections

ARCHITECTURE Struct OF MyLogic IS  
  
 COMPONENT And2 IS  
 PORT (x, y: IN std\_logic;  
 f: OUT std\_logic);  
 END COMPONENT;  
  
 COMPONENT CustomHW IS  
 PORT (x: IN std\_logic;  
 f: OUT std\_logic);  
 END COMPONENT;  
  
 SIGNAL n1, n2: std\_logic;  
  
BEGIN  
 And2\_1: And2 PORT MAP (i0, i2, wire\_1);  
 And2\_2: And2 PORT MAP (wire\_2, i1, d);  
 CustHW: CustomHW PORT MAP (wire\_1, wire\_2);  
END Struct;